Amendments to the Specification:

Please replace paragraph [31] with the following amended paragraph:

[031] The invention provides a device design and corresponding microfabrication process sequence that enables very high yield production of devices or structures requiring a narrow gap between conducting electrodes. This device design and process sequence is particularly well-suited for the fabrication of Charge-Coupled Devices (CCDs) employing a single CCD gate level. The microfabrication process sequence of the invention provides the distinct advantage of producing single gate level CCD structures with a high fabrication yield. Such a high-yield, single-gate-level CCD process is particularly valuable both from the point of view of microfabrication process simplicity as well as CCD device performance, as discussed in detail below. The discussion below focuses on a single-gate-level CCD design and process, but it is to be understood that this is provided as an example only, and that the invention is not limited to such. Additional device and structure designs are contemplated by the invention, as described below.

Please replace paragraph [40] with the following amended paragraph:

[040] In an example fabrication process for producing the single-level gate CCD structure of the invention, a silicon substrate is provided, upon which is grown or deposited a gate dielectric film or films. Such films can consist of, e.g., SiO_2 grown at high temperatures on the wafer in an ambient of O_2 or H_2O, and can include additional deposited layers, e.g., of Si_3N_4 or SiO_2, as desired for a given application. In one example process, a composite-material gate dielectric is produced as a 30 nm-thick thermal SiO_2 layer, a deposited 20 nm-thick Si_3N_4 layer, and a deposited 10 nm-thick SiO_2 layer. Conventional oxide growth and

nitride and oxide deposition techniques can be employed as are well known in the art.

Please replace paragraph [63] with the following amended paragraph:

[063] As discussed above, it is preferable in accordance with the invention to design the process sequence with consideration for the extent to which a dopant introduced in the central region of a gate structure will diffuse to flanking end regions of the gate structure. Referring to Fig. 5A, to investigate this issue, a test pattern 50 was fabricated, consisting of polysilicon layers 52 overlying a dielectric layer 54 on a silicon substrate 56. The polysilicon layer was patterned into strips each having dopant-implanted regions 58 separated by a central, narrow non-implanted region 60 of extent L, as shown in Fig. 5A.